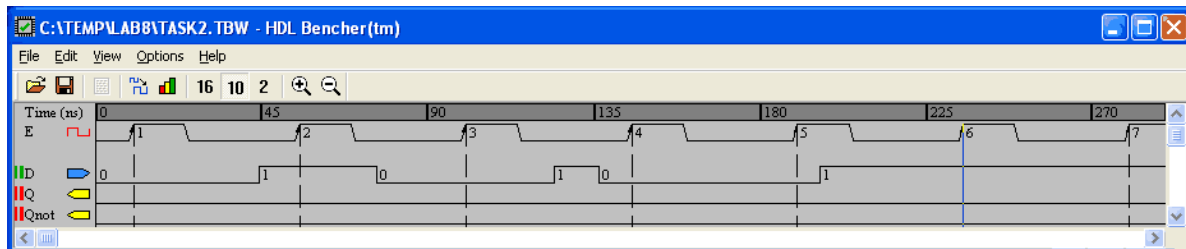
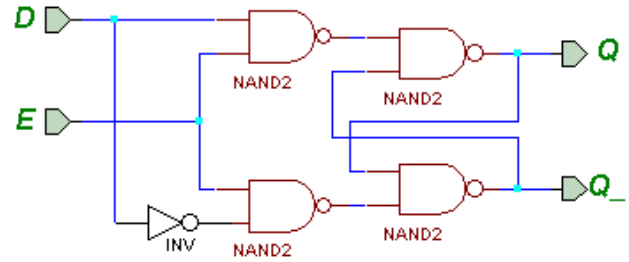




## Task Two: D-Latch with Enable

1. Draw the **D-latch with Enable** circuit in your lab notebook, and build it in the **Xilinx Schematic editor**, using inputs **E** and **D** and outputs **Q** and **Qnot**. This circuit stores a data input under the control of an enable signal.
2. Download the D-latch into the Digilent board, using the same ucf designations as before. Derive a truth table for the D-latch, showing where the *Reset*, *Set* and *NC* modes of operation begin to take place.
3. Exercise the **E** and **D** inputs of the D-latch and try to replicate the input waveforms shown below as well as to generate the simulated outputs. Record this data in your lab notebook. Mark the positions where the *Reset*, *Set* and *NC* modes of operation start on the waveforms. Notice that when **E** is low, the latch is put into a *NC* state.



### Task Three: SRAM Design

We are going to build a 4 word, 4 bit memory (4 x 4) from an array of D-latches. The block diagram of the 4 x 4 memory is shown below. Here are the pertinent inputs and outputs:

- a) 4 data inputs/outputs:  $D_3-D_0$
- b) 2 address inputs:  $A_1 A_0$
- c) 1 write enable:  $WE$

The memory will operate as follows: For a write operation, the  $WE$  (write enable) line is set high and data specified by  $D_3-D_0$  is moved into a word location selected by the decoder. For a read operation,  $WE$  is first set low, and a memory word is selected. The data output may then be read from  $D_3-D_0$ . To allow  $D_3-D_0$  to handle both read and write data transfers, special **tri-state logic buffers** are employed at the output port, as shown in the memory block diagram.

Using the block diagram of the 4-bit memory system given below, complete a logic schematic and download your design in *Xilinx* for your memory as follows:

1. The blue square cell positions contain a **D-Latch**. The  $D$ ,  $E$  and  $Q$  signals should be connected to the blue data line  $D_i$ , the orange write-enabled select line and green **MUX** data line respectively.
2. The orange square logic enables the write enable to pass to one row of D-latches. The orange box should contain an **AND** gate.
3. Now construct this memory as per instructions from the instructor. (You will need to first enlarge the size of the schematic window.)
4. Download the memory design into the PLD and test the operation of your memory by first writing some 4-bit data into each of the 4 memory locations, followed by reading the contents of each of the locations back. Show these results to your lab instructor.

