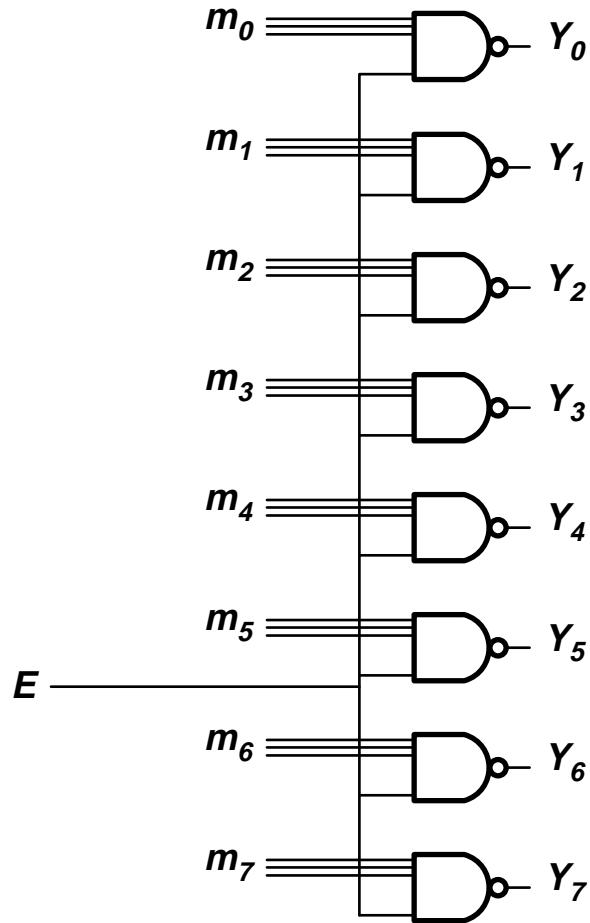
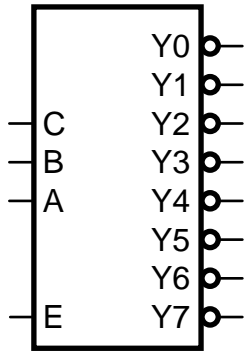
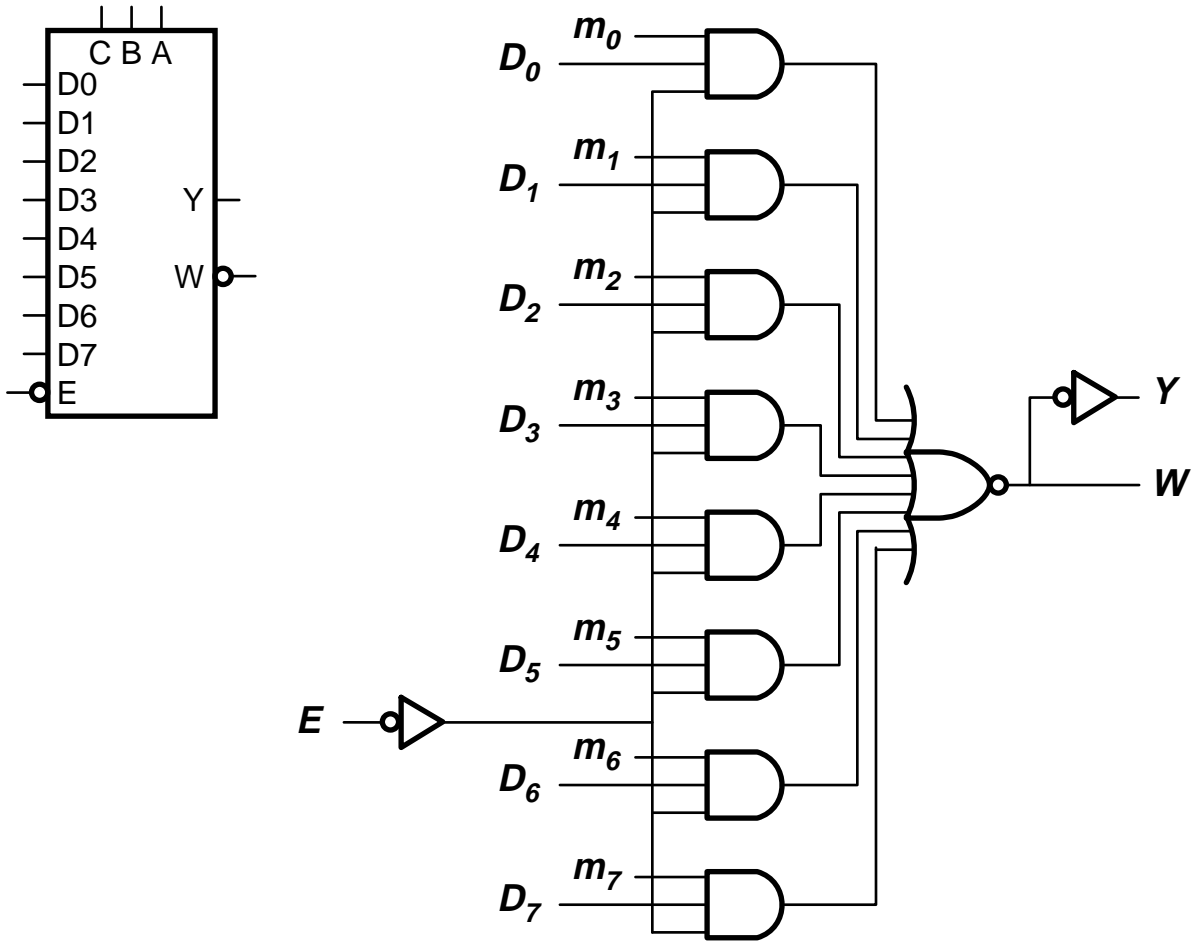


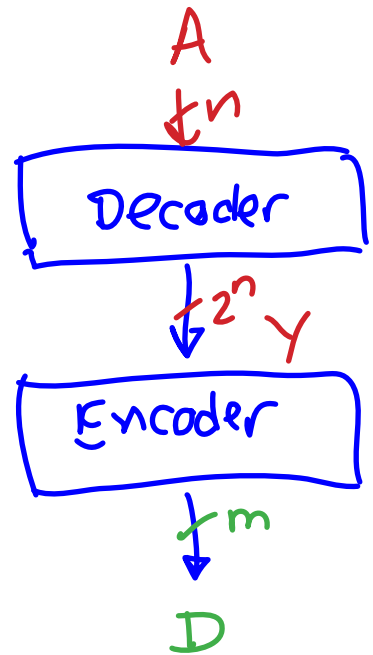
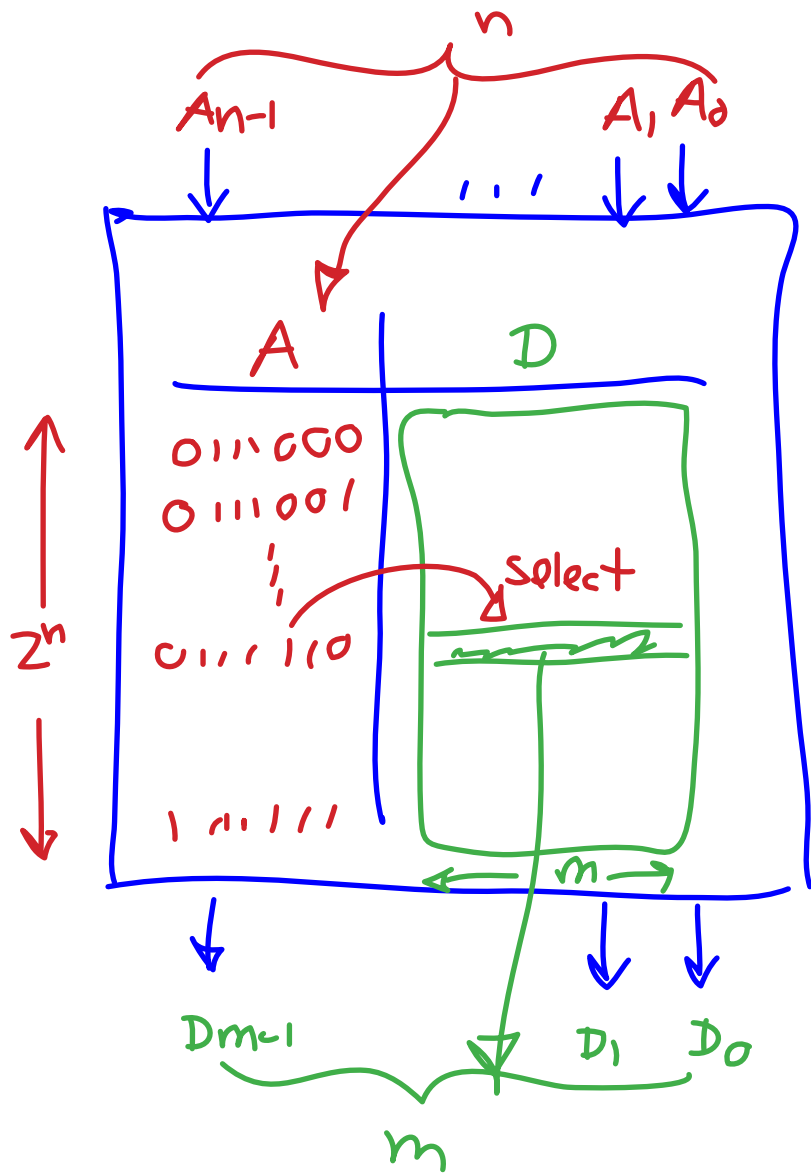
# 3-line to 8-line Decoder



## 8-line to 1-line MUX:

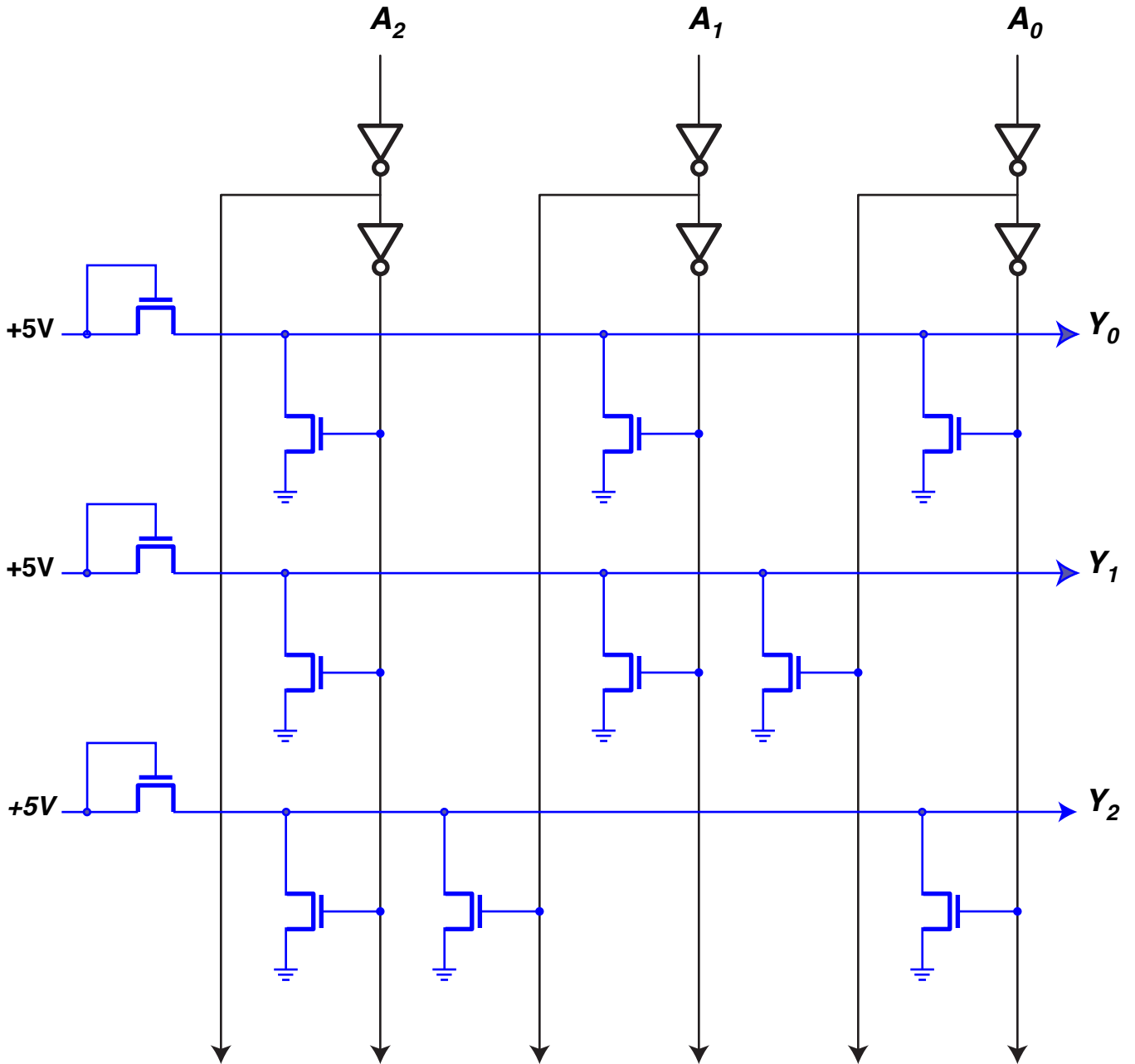


ROM: stores a truth table

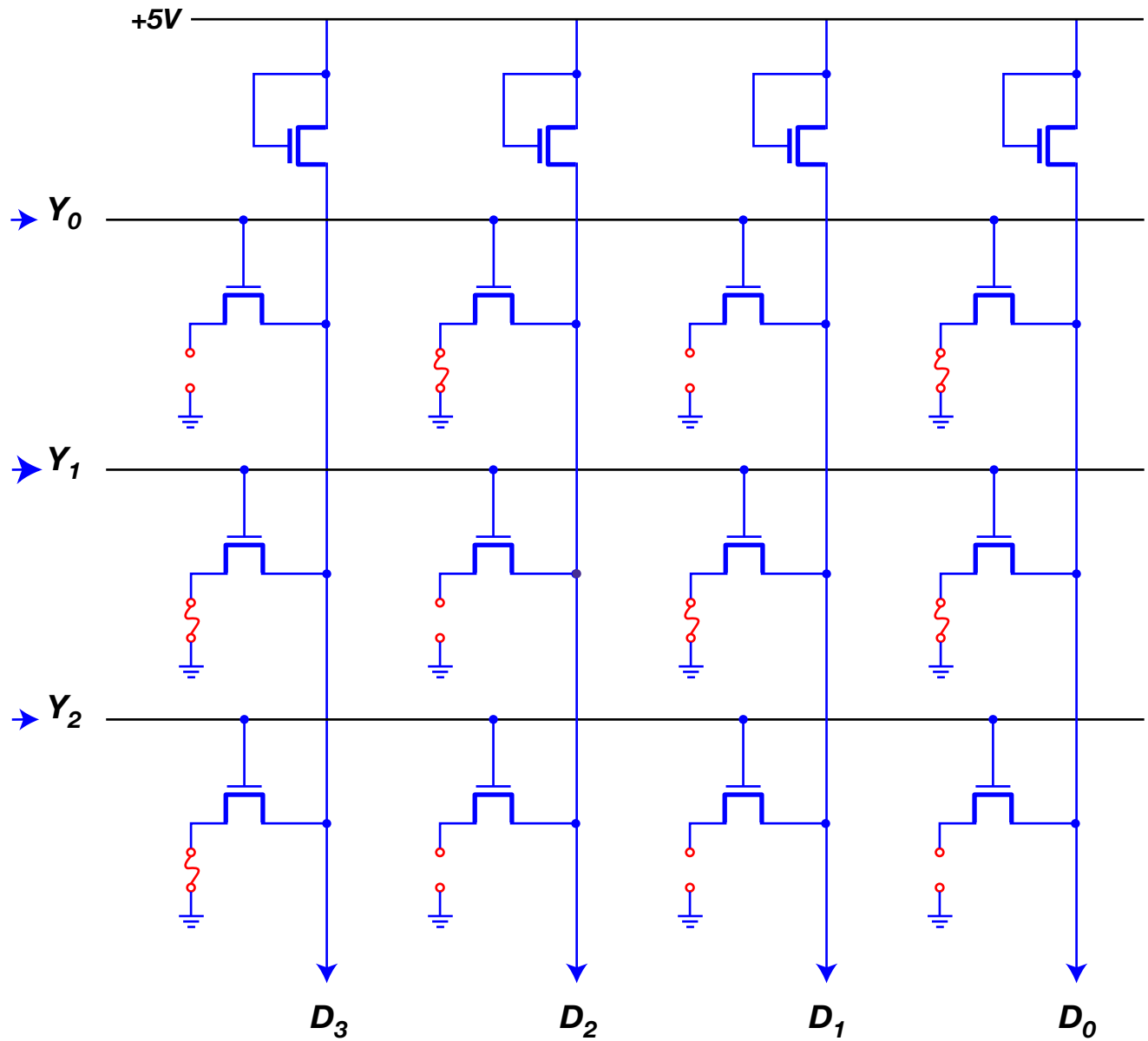


$$C \equiv 2^n \times m$$

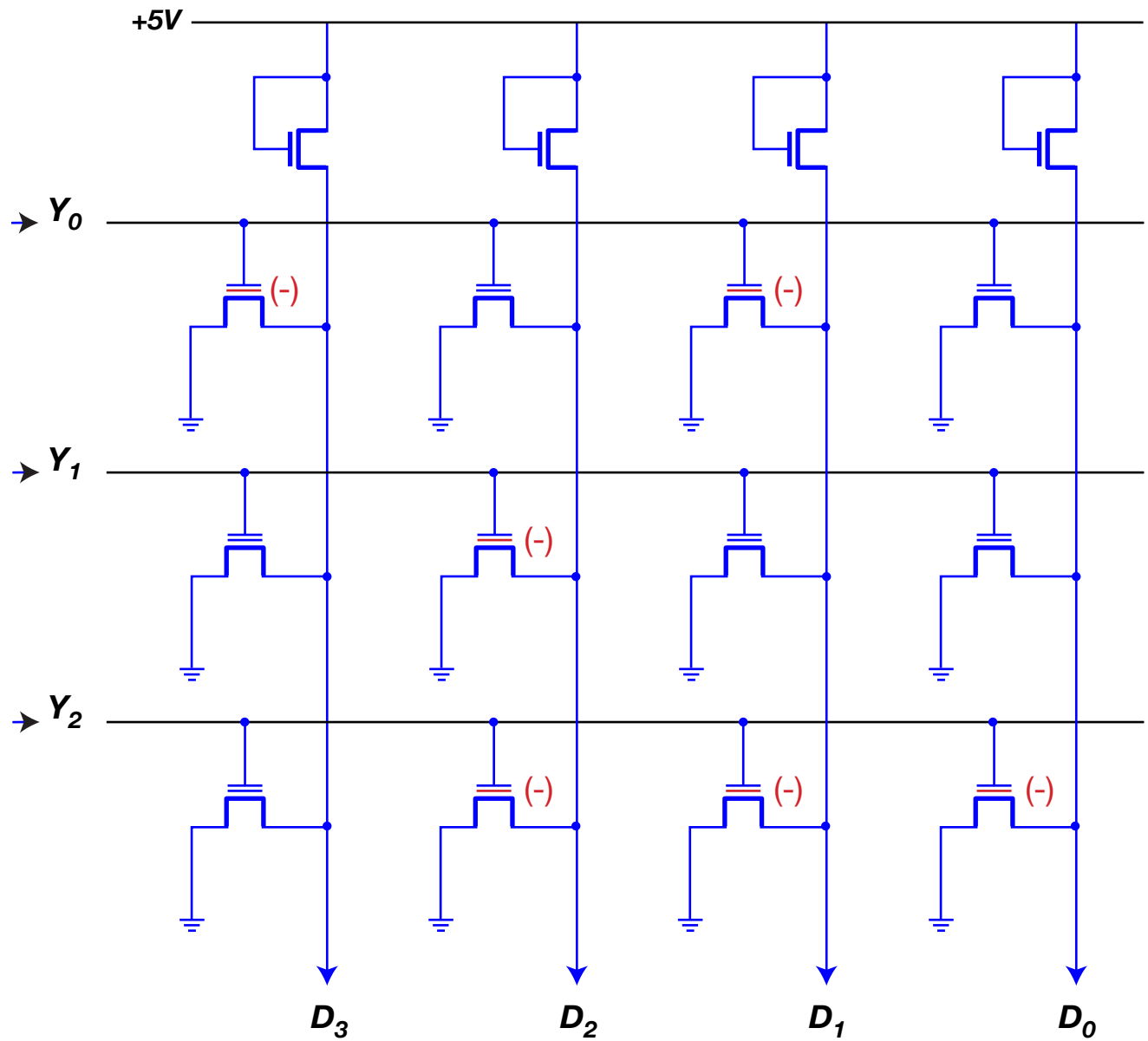
# ROM NMOS Decoder



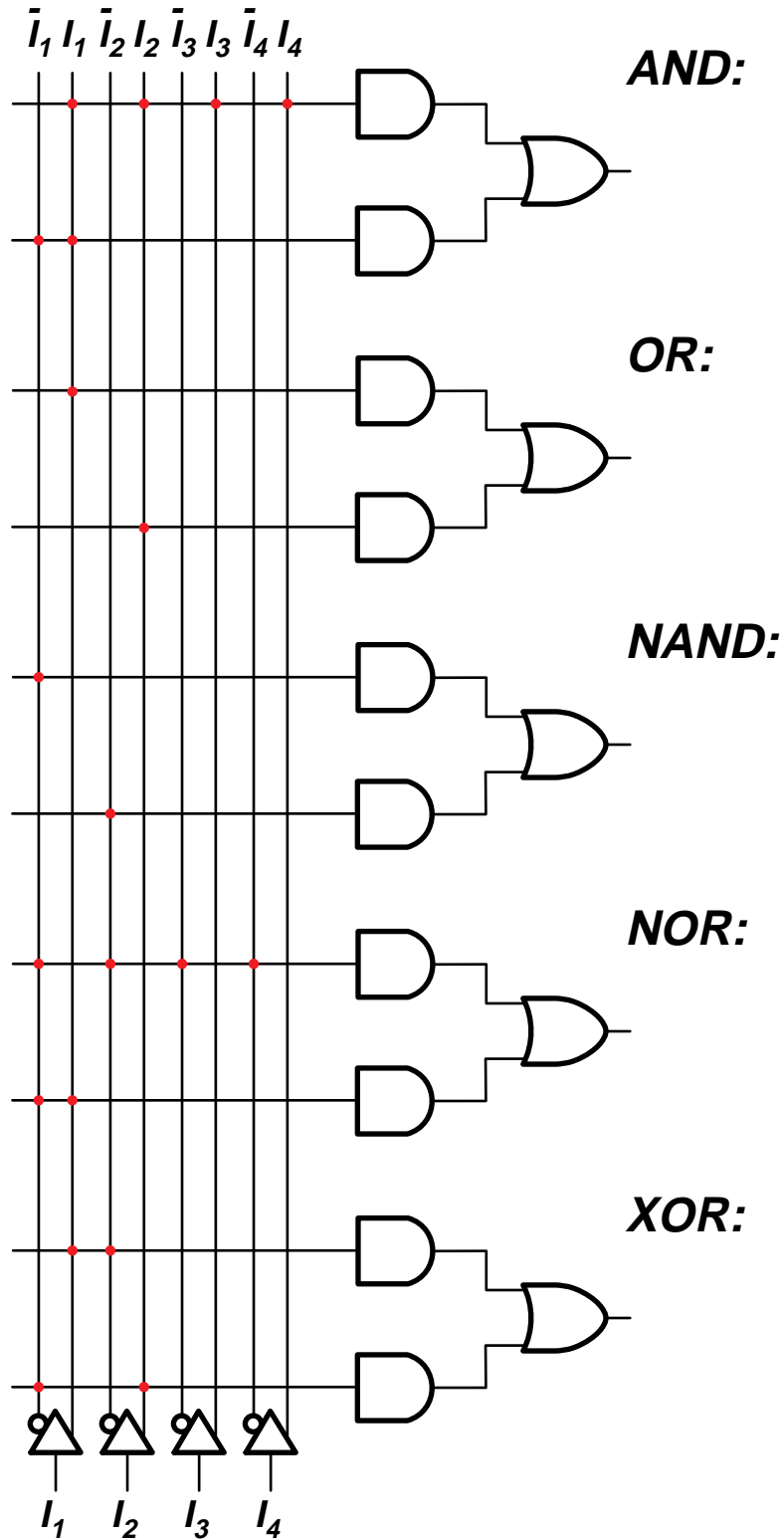
# ROM NMOS Encoder



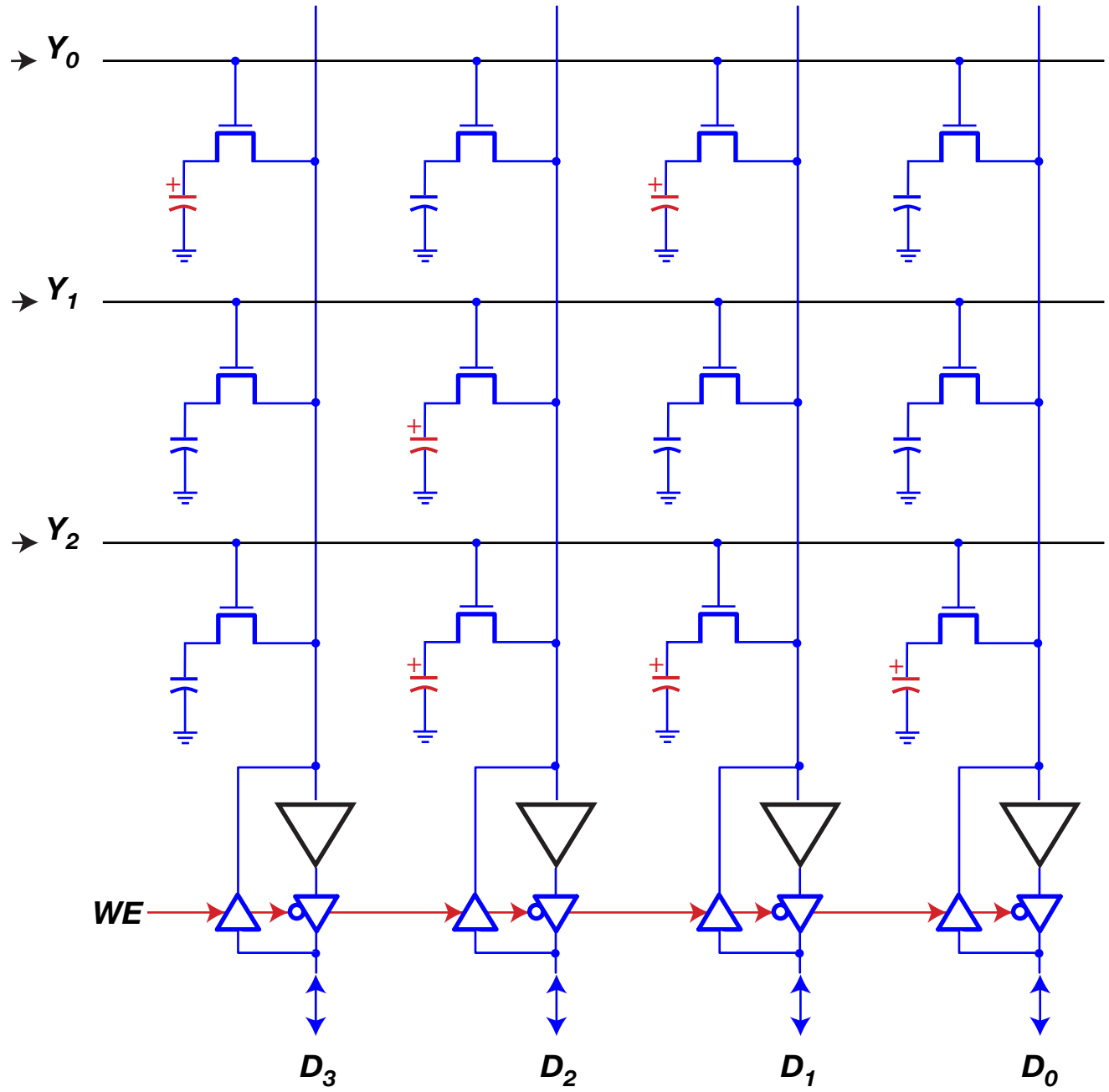
# ***EPRM Encoder w/ Floating Gates***



## 2 x 8 PLD AND Array Examples

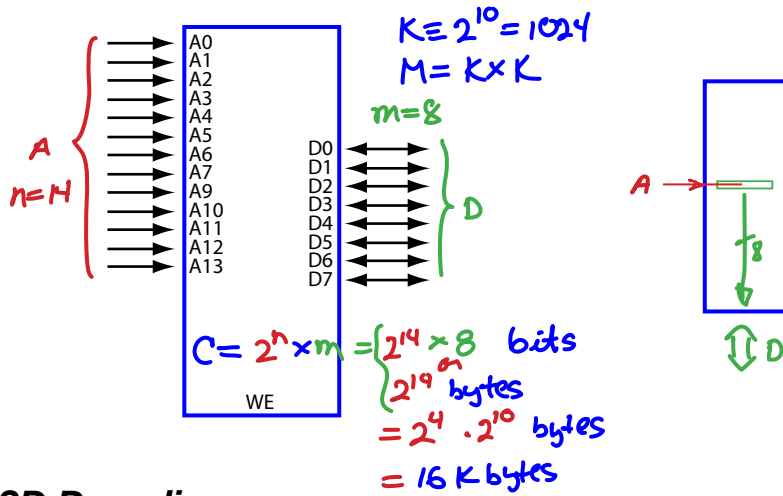


# RAM NMOS Encoder

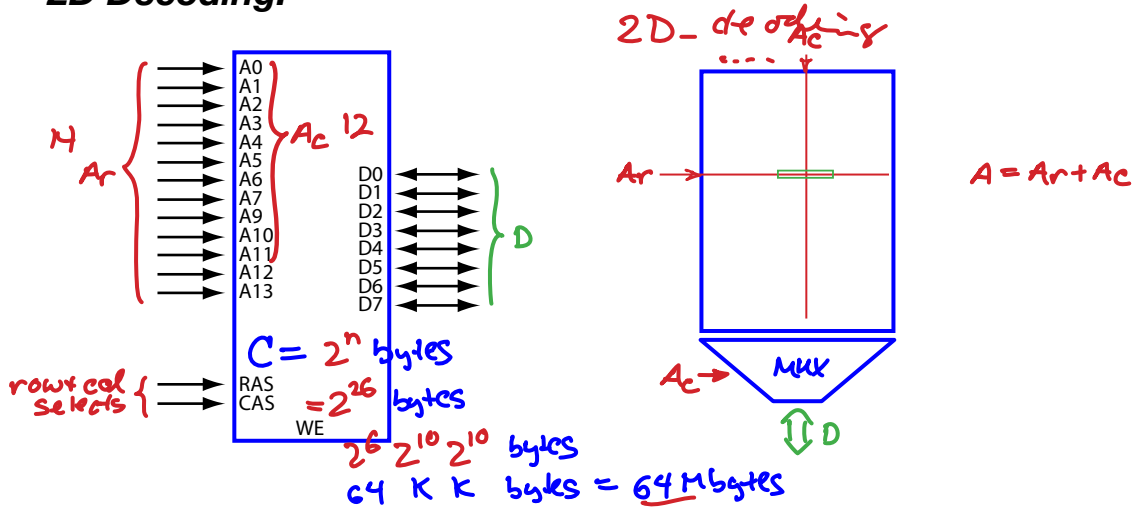


# RAM Chip Addressing

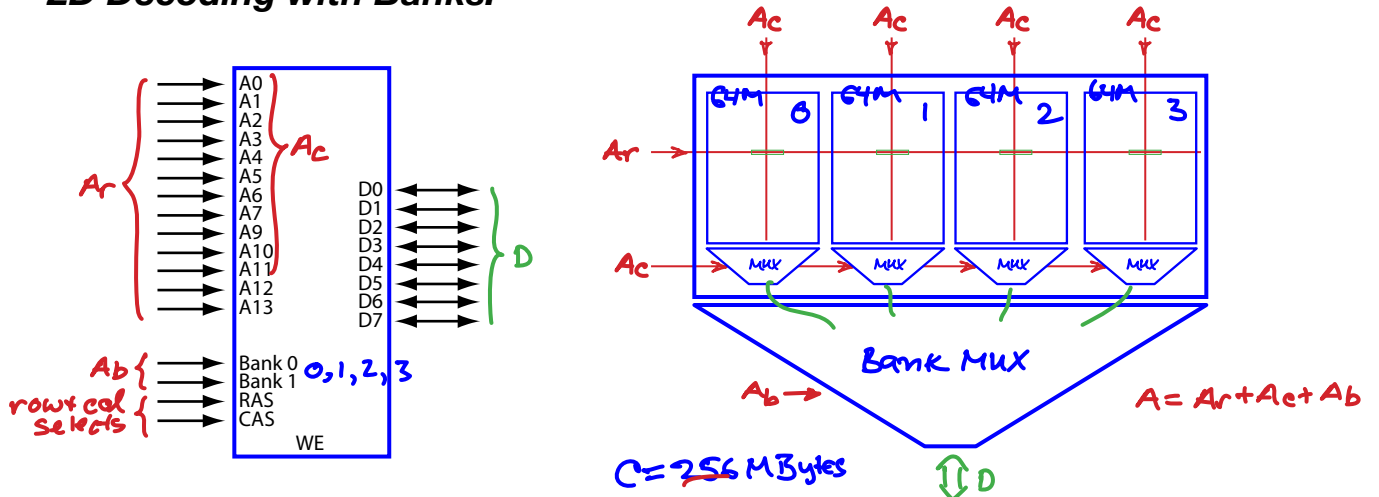
## Straight Decoding:



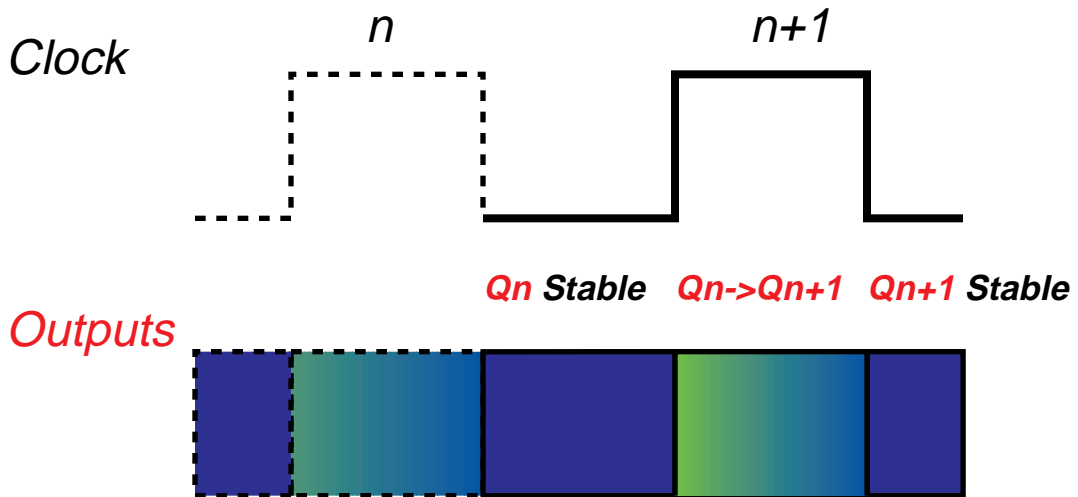
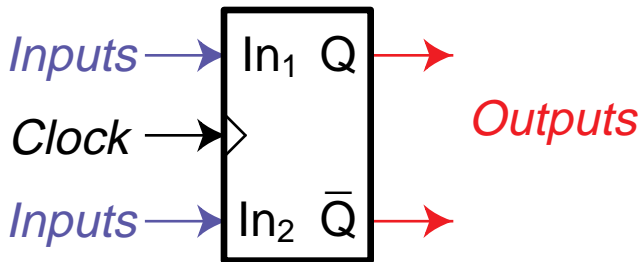
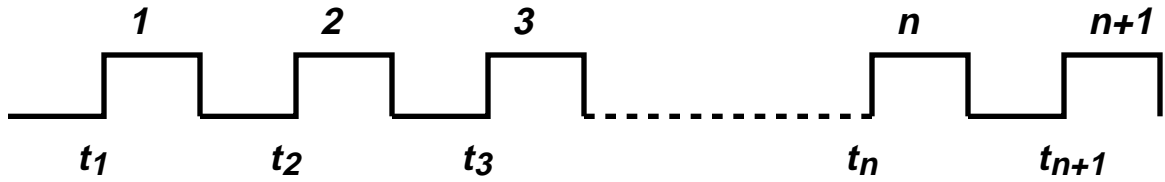
## 2D Decoding:



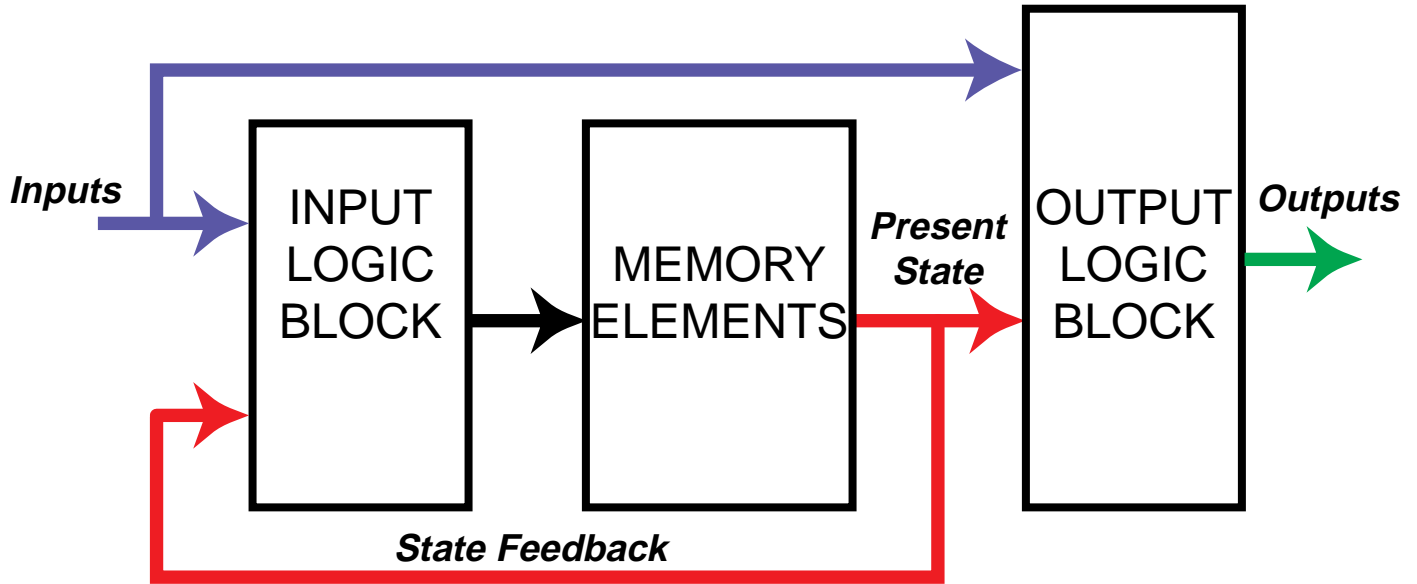
## 2D Decoding with Banks:



# Clock WaveForm Illustrations

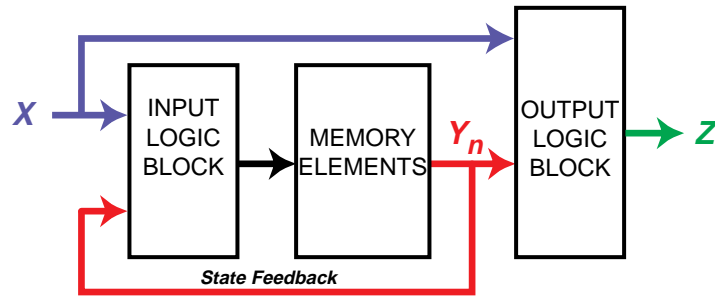


# ***Sequential Logic Circuit Block Diagram***

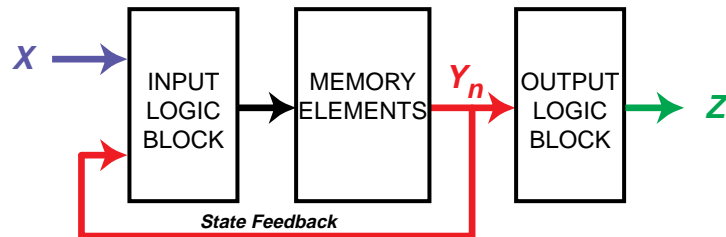


# Sequential Logic Circuit Classes

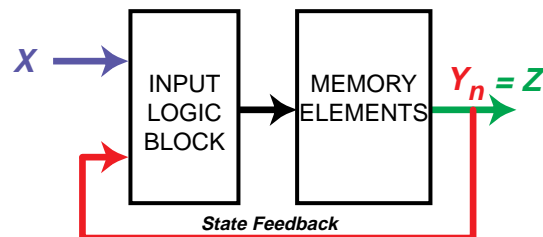
**Class A SLC:  $Z = f(X, Y)$**



**Class B SLC:  $Z = f(Y)$**

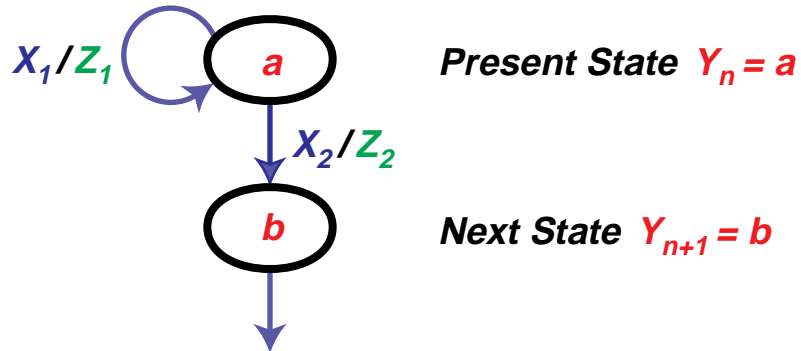


**Class C SLC:  $Z = Y$**



# State Diagrams and Tables

**State Diagram:**

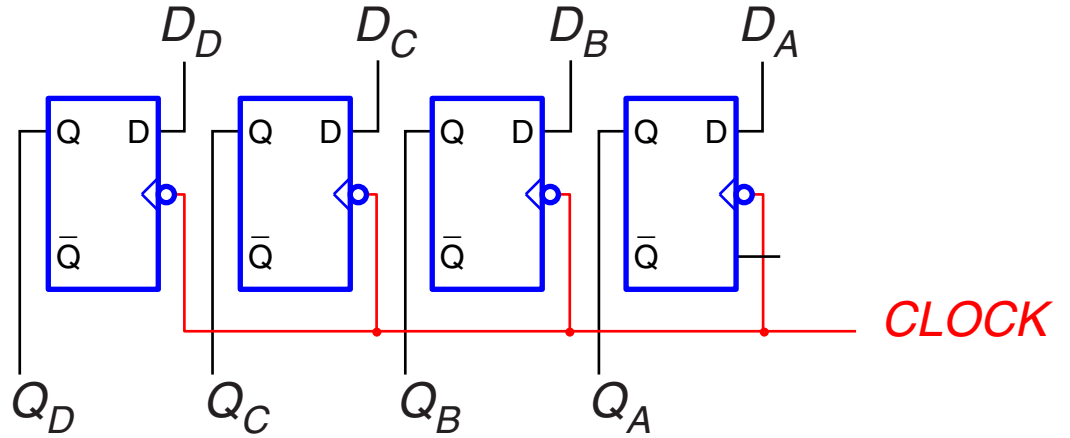


**State Table:**

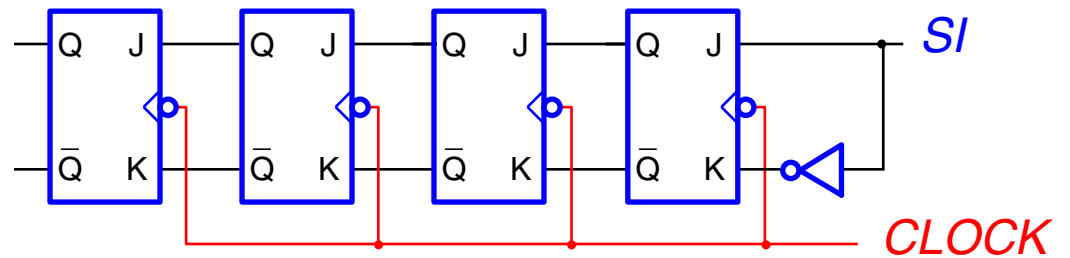
<i>PS</i>	<i>In</i>	<i>NS</i>	<i>Out</i>	
$Y_n$	$X$	$Y_{n+1}$	$Z$	
$a$	$X_1$	$a$	$Z_1$	No Change
$a$	$X_2$	$b$	$Z_2$	Advance to $b$

# Important Types of SLCs

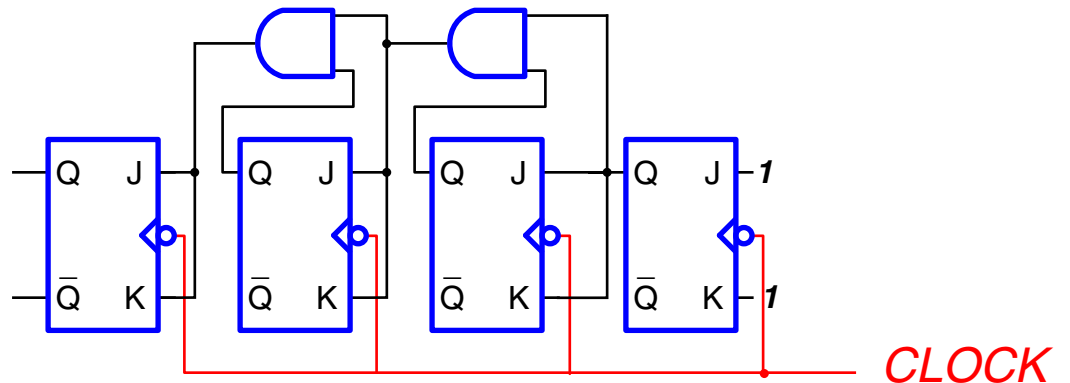
Data Register:



Shift Register:



Synchronous Counter:



Ripple Counter:

